REMARKS

Claims 1-37 have been examined, with all claims remaining rejected under 35 USC 102(e) as being anticipated by Subramanian et al. (2002/0015401; hereinafter, "Subramanian I"), and also remaining rejected under 35 USC 102(e) as being anticipated by Subramanian et al. (2002/0031166) (hereinafter, "Subramanian II"). Applicant continues to traverse these rejections for the reasons set forth below.

Preliminarily, Applicant thanks the Examiner for providing more specific comments regarding which portions of Subramanian I and Subramanian II he believes the claimed features to be taught. These comments have enabled Applicant to more specifically address the Examiner's rejections.

The present invention is directed to a channel CODEC processor 104 having an algorithm-specific kernel block 212-218, 252-258 and a processor core 210, 250. See Figs. 1 and 2. The algorithm-specific kernel block 212-218, 252-258 is operable to receive a data stream, and includes logic tailored to perform at least one step of a channel CODEC algorithm on the data stream. The processor core is coupled to provide configuration data to the algorithm-specific kernel block, wherein the configuration data causes the kernel block to perform the at least one step of the channel CODEC algorithm according to one of a plurality of wireless communication standards as specified by the configuration data.

As explained in the previous Response, both Subramanian I and Subramanian II are assigned to the assignee of the present application, Infineon Technologies AG. Neither of these applied references teaches or even suggests the claimed channel CODEC processor. That is, neither of these references teaches a channel CODEC processor having a processor core that provides an algorithm-specific kernel block with configuration data, as required by the claimed invention.

Before specifically explaining why the applied references do not teach a channel CODEC processor having processor core, it may be helpful to first identify corresponding figures in the application and the two references (i.e., Subramanian I and Subramanian II). As mentioned above,

the application and applied references are all assigned to Infineon Technologies, and as a result the figures have similar layouts. Fig. 1 of the present application shows an electronic communication device, as does Figs. 1B in each of Subramanian I and Subramanian II. Each of these figures includes a configurable channel codec processor 104, and a processor (DSP/μp) 112. Fig. 2 of the present application shows the details of the configurable channel codec processor 104, which includes the claimed processor core 210, 250; there is no such corresponding figure in either of Subramanian I and Subramanian II.

On pages 12 and 13 of the Office Action the Examiner specifically states that he believes each of Subramanian I and Subramanian II teaches the claimed processor core of the channel CODEC to be the processor (DSP/μp) 112. This processor 112 is shown in each of the corresponding figures of the present application and Subramanian I and Subramanian II. However, this processor 112 can not be the claimed processor core 210, 250 because it is not located in the channel CODEC processor 104, as required by the claimed invention. Fig. 2 of the present application shows the details of the channel CODEC processor 104, which includes the claimed processor core 210, 250. Subramanian I and Subramanian II do not show such a processor core located in the channel CODEC processor 104. Thus, the claims are patentable over the applied references for at least this reason.

Further, contrary to the Examiner's statements on pages 12 and 13 of the Office Action, Subramanian I and Subramanian II do not disclose an algorithm specific kernel block at 102a and 104. In Subramanian I and Subramanian II, and also in the present application, reference numeral 102a instead represents a modem processor, and reference numeral 104 represents a channel CODEC processor. (See Fig. 1 of the present application, and Fig. 1B in each of Subramanian I and Subramanian II.) The claimed algorithm specific kernel blocks 212-218, 252-258 are located within the channel CODEC processor 104, as illustrated in Fig. 2 of the present application; again, there is no such corresponding figure in either of Subramanian I and Subramanian II.

In view of the above, Application respectfully submits that the claimed invention is patentable over the applied references. This application is therefore believed to be in condition for allowance. The issuance of a Notice of Allowance is therefore respectfully requested.

Dated: March 9, 2006

Respectfully submitted,

By Laura C. Brutman

Laura C. Brutman
Registration No.: 38,395
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(212) 527-7700
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant